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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,380	12/03/2003	Calvin T. Gabriel	H1604	5577
45305	7590	10/14/2005	EXAMINER	
RENNER, OTTO, BOISSELLE & SKLAR, LLP (AMDS)			TRAN, LONG K	
1621 EUCLID AVE - 19TH FLOOR			ART UNIT	
CLEVELAND, OH 44115-2191			PAPER NUMBER	
			2818	

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/726,380	Applicant(s) GABRIEL ET AL.	
	Examiner Long K. Tran	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 August 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 - 6 is/are pending in the application.
- 4a) Of the above claim(s) 7 - 20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5 and 6 is/are rejected.
- 7) ☒ Claim(s) 4 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>03/28/05</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of group I, claims **1 – 6** in the reply filed on August 08, 2005 is acknowledged.

Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Claims **7 – 20** withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected group II, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on August 08, 2005.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim **1, 2, 3, 5 and 6** are rejected under 35 U.S.C. 102(b) as being anticipated by Avanzino et al. (US Patent no. 6,137,126).
5. Regarding claim **1**, Avanzino discloses a method of fabricating a semiconductor device comprising the steps of:

forming a gate dielectric layer **14** (fig. 1) on a semiconductor substrate **12** (fig. 1);

forming a gate electrode 16 (fig. 1) over the gate dielectric layer 14 wherein the gate electrode 16 defines a channel interposed between source/drain regions 13/13' (fig. 1) formed within an active region of the semiconductor substrate; and

forming contact etch resistant spacers 20 (fig. 1) on sidewalls 15 (fig. 1) of the gate electrode 16 and sidewalls of the gate dielectric layer 14, the contact etch resistant spacers being of a non-silicon oxide and a non-nitride material (SiC; column 3, lines 59 – 67 and column 4, lines 1 – 8 and lines 43 – 46).

Regarding claim 2, Avanzino discloses forming the contact etch resistant spacers 20 includes the steps of:

forming a contact etch resistant layer (not shown; column 4, lines 37 – 43) on the sidewalls 15 of the gate electrode 16, the sidewalls 15 of the gate dielectric 14 and portions of the upper surface (not labeled) of the semiconductor substrate 12; and

etching the contact etch resistant layer to form the contact etch resistant spacers 20 (column 4, lines 43 – 46).

Regarding claim 3, Avanzino discloses forming the contact etch resistant layer of at least one of silicon carbide.

Regarding claim 5, Avanzino discloses forming inter-level dielectric layer 21 (fig. 1; column 2, lines 60 – 61 and column 4, lines 35 – 36) over the contact etch resistant spacers 24 of SiO_x.

Regarding claim 6, Avanzino discloses etching a contact aperture or opening in the inter-level dielectric layer 21 exposing a source/drain (column 2, lines 62 – 63).

Avanzino does not explicitly shows a step of forming a contact mask over the inter-level dielectric layer 21.

However, it is known in the semiconductor technology that to etch a dielectric layer for forming an aperture or opening therein, one partisan in the art would forming a contact mask over the inter-level dielectric layer, patterning the contact mask layer (imaging and developing) then etching the inter-level dielectric layer. Reference to Uehara et al. (US Patent No. 6,713,826; mask 74 (fig. 5(d)); column 11, lines 59 – 67) is cited for the purpose of showing this fact, but not used in the rejection. Thus Avanzino process of fabricating a semiconductor device reads on the claimed forming a contact mask over the inter-level dielectric layer.

Allowable Subject Matter

6. Claim 1 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is an examiner's statement of reasons for the indication of allowable subject matter: Claim 1 is allowable over the prior art of record because none of the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach:

a liner layer of at least one of Si_xN_y and SiO_xN_y formed over the contact etch resistant spacers.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

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accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Tran

October 11, 2005

A handwritten signature in black ink, appearing to read 'L. TRAN', is written over two horizontal lines.